AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 1, lines 5 through 12, with the following paragraph:

(Currently amended) In the current state of integrated circuit technology, there are at least two types of data input signaling modes, single-ended signaling mode and differential signaling mode. Currently, for a variety of reasons, the former tends to be favored by the lower speed, higher voltage integrated circuits, while the later tends to be favored by the higher speed, lower voltage integrated circuits. The differences between the two signaling modes create difficulties for designing the ~~I~~input sections of the integrated circuits of the different types, especially since they often have to co-exist and co-operate with each other in the same system.

Please replace the paragraph on page 2, lines 18 through 22, with the following paragraph:

(Currently amended) Embodiments of the present invention include but are not limited to a micro-architecture for an input section of an integrated circuit (IC), such as a CPU and/or a Chipset, that may be configured to support either differential or single-ended signaling mode of source synchronous data transfer/signaling, ICs having such input sections, and systems having such ICs.

Please replace the paragraph starting on page 3, line 22, and ending on page 4, line 6, with the following paragraph:

(Currently amended) An enabling pulse clock generator **24** may be employed to provide latch banks **26** with enabling pulse clocks **28** to control their operations. The enabling pulse clock generator **24** may provide enabling pulse clocks **28** in accordance with at least strobe signals P **20** and N ~~**20 and**~~ **22**. As will be described in more detail below, enabling pulse clock generator **24** may be designed to be configurable (e.g. per control signal Diffen) to provide enabling pulse clocks **28** further in accordance with a

selected one of at least the single-ended signaling mode and the differential signaling mode.

Please replace the paragraph on page 4, lines 12 through 16, with the following paragraph:

(Currently amended) Sense amplifier circuits **14** and **16** (two each) are employed to provide strobe signals P **20** and N ~~**20 and**~~ **22** to e<u>E</u>nabling ~~p~~<u>P</u>ulse ~~c~~<u>C</u>lock ~~g~~<u>G</u>enerator **24** for the differential signaling mode and the single-ended signaling mode, respectively. <u>That is, strobe signal P **20** is provided to Enabling Pulse Clock Generator **24** for the differential signaling mode, and strobe signal N **22** is provided to Enabling Pulse Clock Generator **24** for the single-ended signaling mode.</u> Both sense amplifier circuits **14** and **16** provide strobe signals P **20** and N ~~**20 and**~~ **22** in accordance with at least strobe inputs **12**.

Please replace the paragraph starting on page 4, line 22, and ending on page 5, line 2, with the following paragraph:

(Currently amended) Multiplexors **18** are employed to configurably select and provide (e.g. per control signal Diffen) the outputs of sense amplifier circuits **14** and **16** as strobe signals P **20** and N ~~**20 and**~~ **22** for the differential signaling mode and the single-ended signaling mode, respectively.

Please replace the paragraph on page 5, lines 3 through 9, with the following paragraph:

(Currently amended) Configuration of input section **10** may be effectuated in any one of a number of manners, including but ~~are~~ not limited to the setting of one or more control bits in a configuration register (not shown) of the IC, or fusing of one or more fuses (not shown) of the IC. In various embodiments, the configuration register or the fuses may be configured to cause the control signal Diffen to assume a value of "1"

to configure input section **10** to operate in a differential signaling mode, and a value of '0" to configure input section **10** to operate in a single-ended signaling mode.

Please replace the paragraph starting on page 5, line 10, and ending on page 6, line 4, with the following paragraph:

(Currently amended) **FIGS. 2A** and **2B** illustrate input section **10** in further detail, in particular sense amplifier circuits **14** and **16** and latch banks **26**, according to some embodiments of the invention. As described earlier, 16 latch banks **26** are illustrated for the embodiments, the latch banks **26** divided into two groups of even and odd latch banks~~, 104 and 105~~. Further, as illustrated in **FIG. 2B**, for the embodiment, each group of latch banks ~~26~~ contains 8 deskewing latches **106** for capturing bit data received via data paths **27**. As described earlier (regarding latch banks **26**) deskewing latches **106** latch data off data paths **27** in accordance with enabling pulse clocks **28~~6~~**, more specifically, enabling pulse clocks En0 – En15. In various embodiments, a set of enabling pulse clocks En0 – En15 is provided in a predetermined time period, e.g. two bus clock cycles. Moreover, enabling pulse clocks En0 – En15 may be configurably provided in one of at least two manners, a manner suitable for differential signaling and another manner suitable for single-ended signaling. In the former case, enabling pulse clocks En0 – En15 may be provided in 16 points in time during the period, one enabling pulse clock per point in time, whereas in the later case, enabling pulse clocks En0 – En15 may be provided in 8 points in time during the period, two enabling pulse clock per point in time, to be described more fully below.

Please replace the paragraph starting on page 6, line 22, and ending on page 7, line 6, with the following paragraph:

(Currently amended) As also illustrated in **FIG. 2A**, for the embodiment, each of sense amplifier circuits **16** includes sense amplifier **118** and **120**, whereas each of sense amplifier circuits **14** includes sense amplifier **114** and **116**. In the former case, each of sense amplifiers **118/120** receives one of the two strobe signals, and a Gunning

Transceiver Logic ("GTL") signal (GTLREF) as a reference signal, and generates StbP/StbN based on the received signals. In the latter case, each of sense amplifiers **114 and 116** receives both two strobe signals, and generates StbP/StbN based on the received signals (in opposite manners).

Please replace the paragraph on page 8, lines 9 through 11, with the following paragraph:

(Currently amended) For the embodiment of **FIG. 3**, enabling pulse clock generator **24** includes add unit **167**, selectors **169**, ring counters **160** and **162**, and two sets of logic elements **170** and **172**, coupled to each other as shown. That is, logic element set **170** comprises the eight AND gates illustrated outputting En0, En2, ...En14, and logic element set **172** comprises the eight AND gates outputting En1, En3, ...En15.

Please replace the paragraph on page 9, lines 5 through 13, with the following paragraph:

(Currently amended) Selectors **169** are employed to output a selected one of the StbN and the identical version, and a selected one of the StbP and the identical version, for ring counters **160** and **162** respectively, depending on the signaling mode (as denoted e.g. by the Diffen signal). More specifically, selectors **169** are employed to output the StbN and StbP signals as StbNFallingEdge and StbPFallingEdge for ring counters **160** and **162** respectively, when configured to operate in the single-end signaling mode, and two streams of the identical version as StbNFallingEdge and StbPFallingEdge for ring counters **160** and **162** respectively, when configured to operate in the differential signaling mode.

Please replace the paragraph starting on page 10, line 18, and ending on page 11, line 6, with the following paragraph:

(Currently amended) **FIG. 5** depicts timing of the various signals when enabling pulse clock generator **24** is configured to operate in the differential signaling

mode according to some embodiments. Similarly, for the illustrated embodiment, each of these timing diagrams **212**, **218**, **220**, **222** and **224** represents a period of two bus clock cycles. In this example, two sets of 8 data bits **212** are to be interleavingly latched and transferred on during the period. When configured to operate in the differential signaling mode, StbPFallingEdge and StbNFallingEdge pulses, **218** and **220** respectively, may be formed based on StbP **204** and StbN **206** as shown. StbNFallingEdge and StbPFallingEdge pulses, **220**~~18~~ and **218**~~20~~ respectively, may then be fed into ring counters **160** and **162** to generate initial enabling pulses **222** (T0 T2..T14 and T1 T3...T15, respectively). These pulses when "AND'd" with the appropriate strobes result in clock pulses **224** (En0 En2 ...En14 and En1 En3 ... En15) at the 16 points in time during the period.

Please replace the paragraph starting on page 11, line 21, and ending on page 12, line 9, with the following paragraph:

(Currently amended) **FIG. 7** is a flow diagram **300** that illustrates a method of the invention, according to some embodiments of the invention. At **302**, strobe signals are received from, for example, an external source. If the input section **10** is configured to operate in single-ended signaling mode, then differential sense amplifiers and squelch detector may be disabled or their outputs may be ignored at **306**. Based on the strobe signals received, StbPFallingEdge/StbNFallingEdge pulses may be generated from the falling edges of StbP and StbN at **308**. Each of the pulse clocks may then be fed into a ring counter to generate initial enabling pulse clocks at **310** (for an 8-bit embodiment, each ring counter may generate 16 enabling pulses in 8 points in time in a period). These enabling pulses may then be "AND'd" with strobes to generate the final enabling pulse clocks at **312**. These enabling pulse clocks may then be sent to the latch banks at **314**.